forming over the second substrate, in inverted order, a dielectric isolated metallization pattern intended to mate with the partially fabricated semiconductor integrated circuit microelectronic fabrication;

laminating the partially fabricated semiconductor integrated circuit microelectronic fabrication with the second substrate to mate the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern to thus form a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication; and

removing the second substrate from the laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a method selected from the group consisting of milling methods, polish methods and chemical mechanical polish (CMP) planarizing methods.

~~11. (amended)~~ The method of claim 1 wherein the chemical mechanical polish (CMP) planarizing method employs the dielectric isolated metallization pattern as a stop layer.

Please cancel claims 9-10.

Please add new claims 14-15 as follows.

14. (newly added) A method for fabricating a semiconductor integrated circuit microelectronic fabrication comprising:

providing a first semiconductor substrate;

forming over the first semiconductor substrate at least one microelectronic device to form from the first semiconductor substrate a partially fabricated semiconductor integrated circuit microelectronic fabrication;

providing a second substrate;

forming over the second substrate, in inverted order, a dielectric isolated metallization pattern intended to mate with the partially fabricated semiconductor integrated circuit microelectronic fabrication; and

pressure laminating the partially fabricated semiconductor integrated circuit microelectronic fabrication with the second substrate to mate the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern to thus form a pressure laminated completely fabricated semiconductor integrated circuit microelectronic fabrication.

15. (newly added) The method of claim 14 wherein the partially fabricated semiconductor integrated circuit microelectronic fabrication and the second substrate are pressure laminated while employing a bonding material selected from the group consisting of indium and indium alloy bonding materials.